Amendments to the Claims:

Claims 10, 11, 25, 28, 31, 33, 34, and 38 have been amended, claims 9 and 12 have been cancelled, and new claims 41 and 42 have been added. This listing of the claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

(Claims 1-9 have been cancelled)

10.(Currently Amended) A ~~The~~ microprocessor ~~of claim 9~~, comprising:

a central processing unit with an instruction set including three-byte instructions~~wherein said instruction set further includes~~, two-byte instructions and one-byte instructions;

a memory for storing the instructions, wherein all of a selected set of the instructions is stored contiguously without any gaps; and

a memory interface for supplying the instructions from the memory to the central processing unit, wherein all bytes of each of said selected instructions are supplied simultaneously in a single fetch operation.

11.(Currently Amended) ~~The~~ microprocessor ~~of claim 9~~, comprising:

a central processing unit with an instruction set including three-byte instructions;

a memory for storing the instructions, wherein all of a selected set of the instructions is stored contiguously without any gaps; and

a memory interface for supplying the instructions from the memory to the central processing unit, wherein all bytes of each of said selected instructions are supplied simultaneously in a single fetch operation, and wherein said memory is a one time programmable memory.

(Claims 12-24 have been cancelled)

25.(Currently Amended) A method of operating a microprocessor, the microprocessor comprising a central processing unit with an instruction set including N-byte instructions, a memory for storing the instructions, and a memory interface for supplying the

instructions from the memory to the central processing unit, wherein N is an integer greater than one, the method comprising:

logically organizing the memory as a plurality rows of M byte-wide columns, wherein M is an integer greater than one and wherein N and M are relatively prime;

programming a selected set of instructions of the instruction set into the memory, wherein all of the selected set of instructions ~~are~~ is stored contiguously without any gaps in the memory; and

operating the interface whereby each of the selected instructions can be supplied simultaneously from the memory to the central processing unit in a single fetch operation.

26.(Previously Presented) The method of claim 25, wherein N is equal to three and M is equal to four.

27.(Previously Presented) The method of claim 26, wherein said instruction set further includes two byte instructions and one byte instructions.

28.(Currently Amended) The method of claim 26, wherein said memory interface comprises a bus on which the selected instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

29.(Previously Presented) The method of claim 25, wherein the memory is an embedded memory of the microprocessor.

30.(Previously Presented) The method of claim 29, wherein the memory is a one time programmable memory.

31(Currently Amended) The microprocessor of claim 10, wherein said memory is four bytes wide.

32.(Previously Presented) The microprocessor of claim 10, wherein said memory is a one time programmable memory.

33.(Currently Amended) A ~~The~~ microprocessor ~~of claim 10~~, comprising:

a central processing unit with an instruction set including three-byte instructions, two-byte instructions and one-byte instructions;

a memory for storing the instructions, wherein the instructions are stored contiguously; and

a memory interface for supplying the instructions from the memory to the central processing unit, wherein all bytes of each of said instructions are supplied simultaneously in a single fetch operation, and wherein said memory interface comprises a bus on which the instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

34.(Currently Amended) A microprocessor, comprising:

a central processing unit operable according to an instruction set including instructions of one-byte, two-byte, and three-byte lengths;

a memory for storing a selected set of said instructions, wherein all of the selected ~~members of the instruction~~ set ~~are~~ is stored contiguously without any gaps; and

a memory interface for supplying instructions of the instruction set from the memory to the central processing unit, wherein each of said instructions is individually suppliable in a single fetch operation in which all bytes of a supplied instruction are supplied simultaneously.

35.(Previously Presented) The microprocessor of claim 34, wherein said memory is organized as a plurality rows of M byte-wide columns, wherein M is an integer greater than three that is not divisible by three.

36.(Previously Presented) The microprocessor of claim 34, wherein said memory is a one time programmable memory.

37.(Previously Presented) The microprocessor of claim 34, wherein said memory interface comprises a bus on which the instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

38.(Currently Amended) The method of claim 27, wherein said memory interface comprises a bus on which the selected instructions are supplied from said memory to the central processing unit and wherein said bus is three bytes wide.

39.(Previously Presented) The method of claim 27, wherein the memory is an embedded memory of the microprocessor.

40.(Previously Presented) The method of claim 39, wherein the memory is a one time programmable memory.

41.(New) The microprocessor of claim 33, wherein the memory is an embedded memory of the microprocessor.

42.(New) The microprocessor of claim 33, wherein the memory is a one time programmable memory.